#innovacion
#ayudascdti
#asesoramiento
#internacionalizacion

Chips JU – WP2025

Enrique Pelayo Campillos, PhD

NCP HE/Digital – CDTI

HORIZONTE
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Index

HE / Cluster 4

Chips-JU

Successful proposal

HE / Cluster 4

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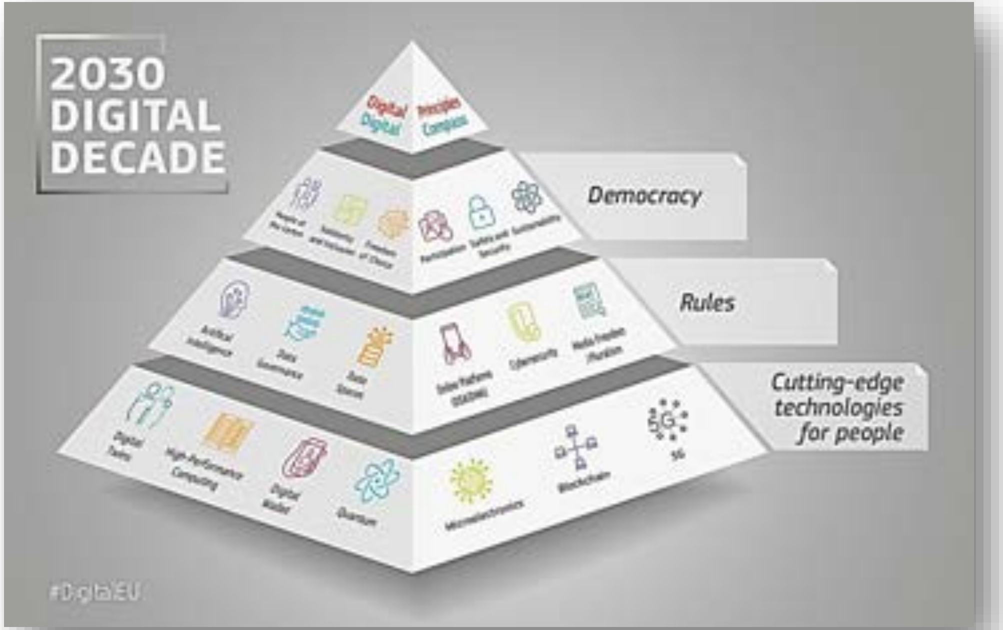
División de Programas de la UE

GOBIERNO DE ESPAÑA
MINISTERIO DE CIENCIA, INNOVACIÓN Y UNIVERSIDADES

CDTI INNOVACIÓN

Estrategia y Políticas Digitales



+


Connectivity


Data


Chips ACT

Advanced computing

• • •

Artificial Intelligence

Horizonte Europa – Clúster 4

Pillar I
EXCELLENT SCIENCE

- European Research Council
- Marie Sklodowska-Curie
- Research Infrastructures

Pillar II
GLOBAL CHALLENGES & EUROPEAN INDUSTRIAL COMPETITIVENESS

Clusters
- Health
- Culture, Creativity & Inclusive Society
- Civil Security for Society
- Digital, Industry & Space
- Climate, Energy & Mobility
- Food, Bioeconomy, Natural Resources, Agriculture & Environment

Joint Research Centre

Pillar III
INNOVATIVE EUROPE

- European Innovation Council
- European Innovation Ecosystems
- European Institute of Innovation & Technology*

WIDENING PARTICIPATION AND STRENGTHENING THE EUROPEAN RESEARCH AREA

- Widening participation & spreading excellence
- Reforming & Enhancing the European R&I system

~ 15.000 M€

Partenariados HE/Digital

Institucionalizados

- Chips (**Chips JU**)
- High Performance Computing (**EuroHPC JU**)
- Smart Networks and Services (**SNS JU**)

Co-programdaos

- AI / Data / Robotics (**ADRA**)
- Photonics
- Virtual Worlds **NUEVO**

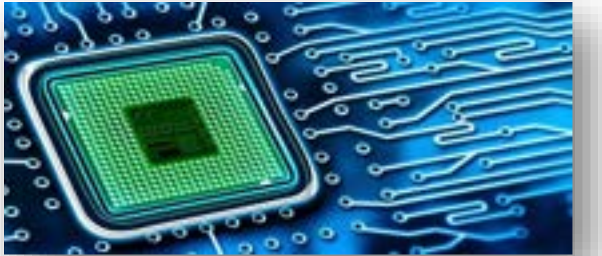
Clúster 4 - Digital

D3 - DATA

Data

Computation Networks

D4 - EMERGING



Quantum

Photonics

Robotics

AI in science

D6 - HUMAN

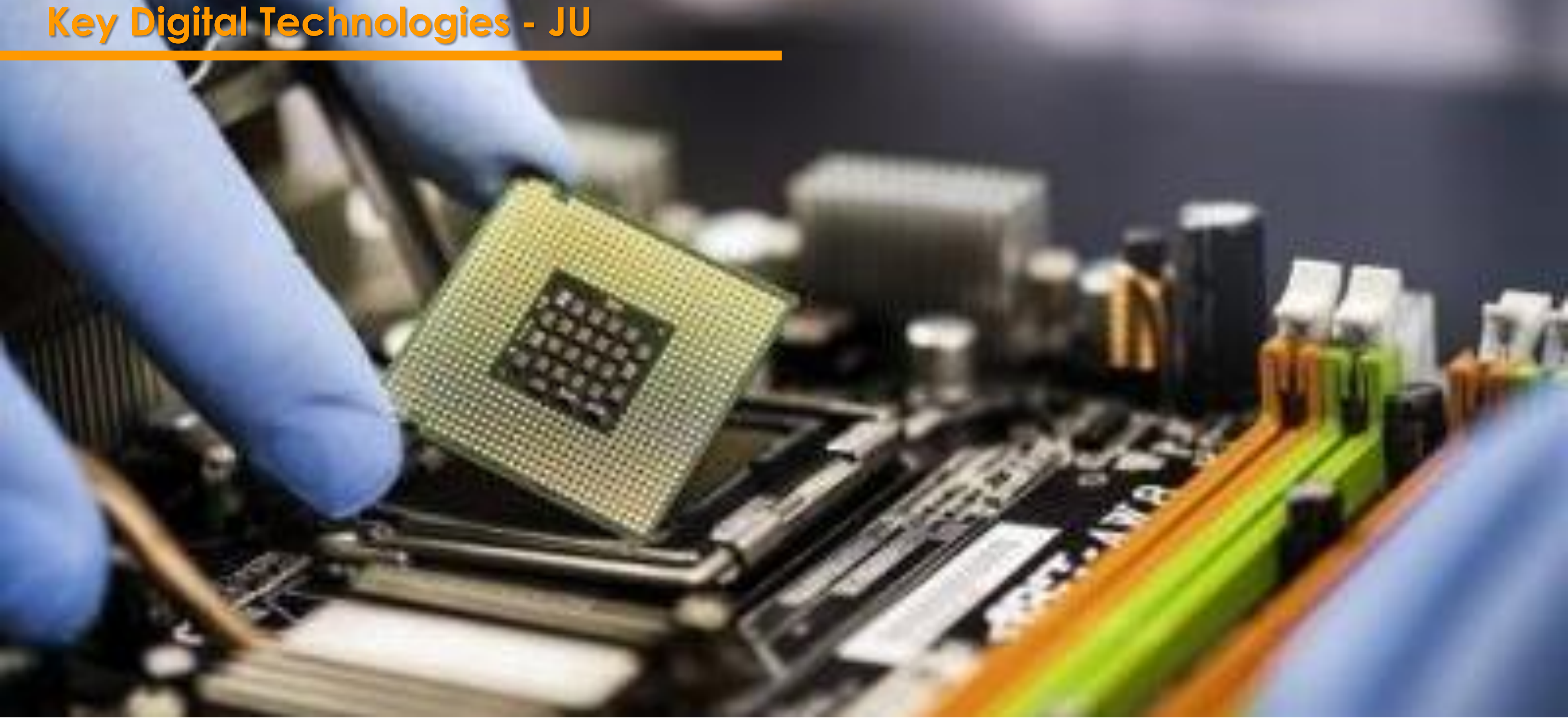
Gen AI

Virtual Worlds

Standard & valorization

International cooperation

Key Digital Technologies - JU



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Estrategia Europea en Semiconductores: Necesidad

Incremento demanda

Cadena suministro frágil
(Dependencia Taiwan/ Corea, problemas geopolítica)

↓

Problemas en industria
(11 M de coches menos fabricados en 2021)

"There is no digital without chips. And while we speak, whole production lines are already working at reduced speed - despite growing demand - because of a shortage of semi-conductors.

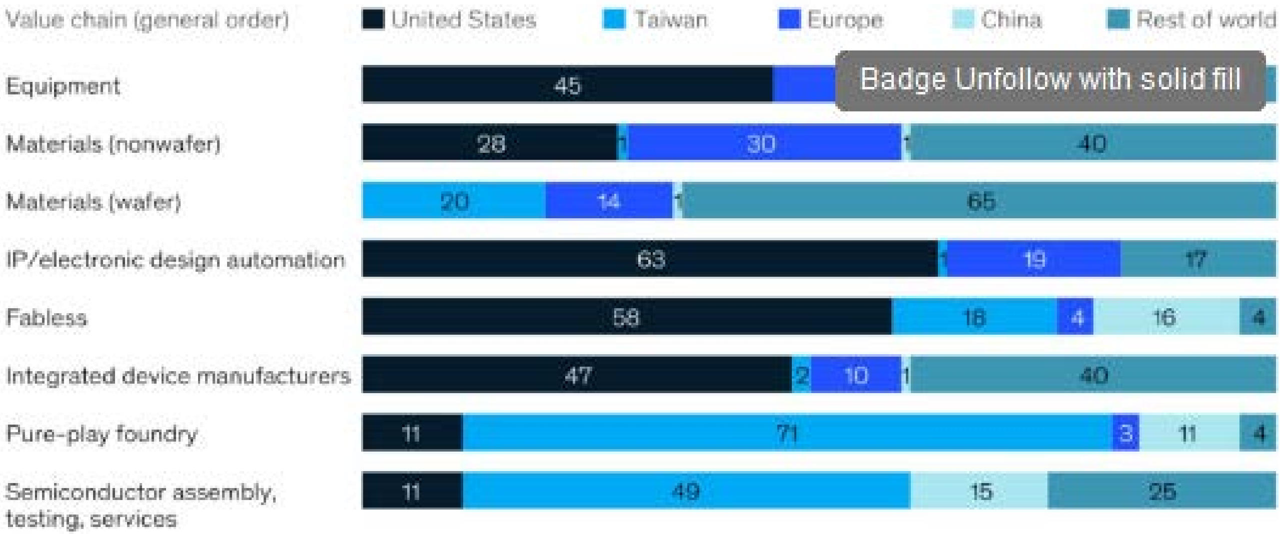
But while global demand has exploded, Europe's share across the entire value chain, from design to manufacturing capacity has shrunk. We depend on state-of-the-art chips manufactured in Asia.

So this is not just a matter of our competitiveness. This is also a matter of tech sovereignty."

--- Ursula von der Leyen, 15/Sept/2021

Estrategia Europea en Semiconductores: Posición UE

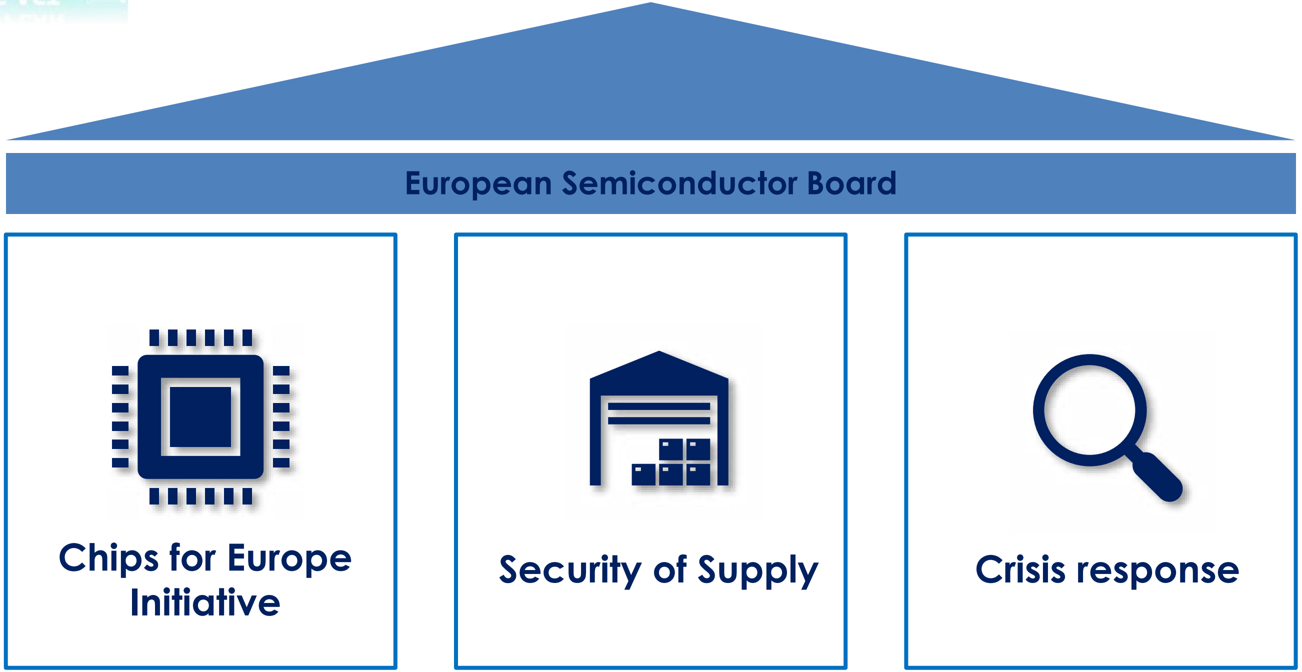
Dependencia UE en: **diseño**, **fabricación** y **empaquetado** de semiconductores



Source: Gartner; IHS; Strategy Analytics; McKinsey

EUROPEAN CHIPS ACT

Políticas Digitales: Chips ACT



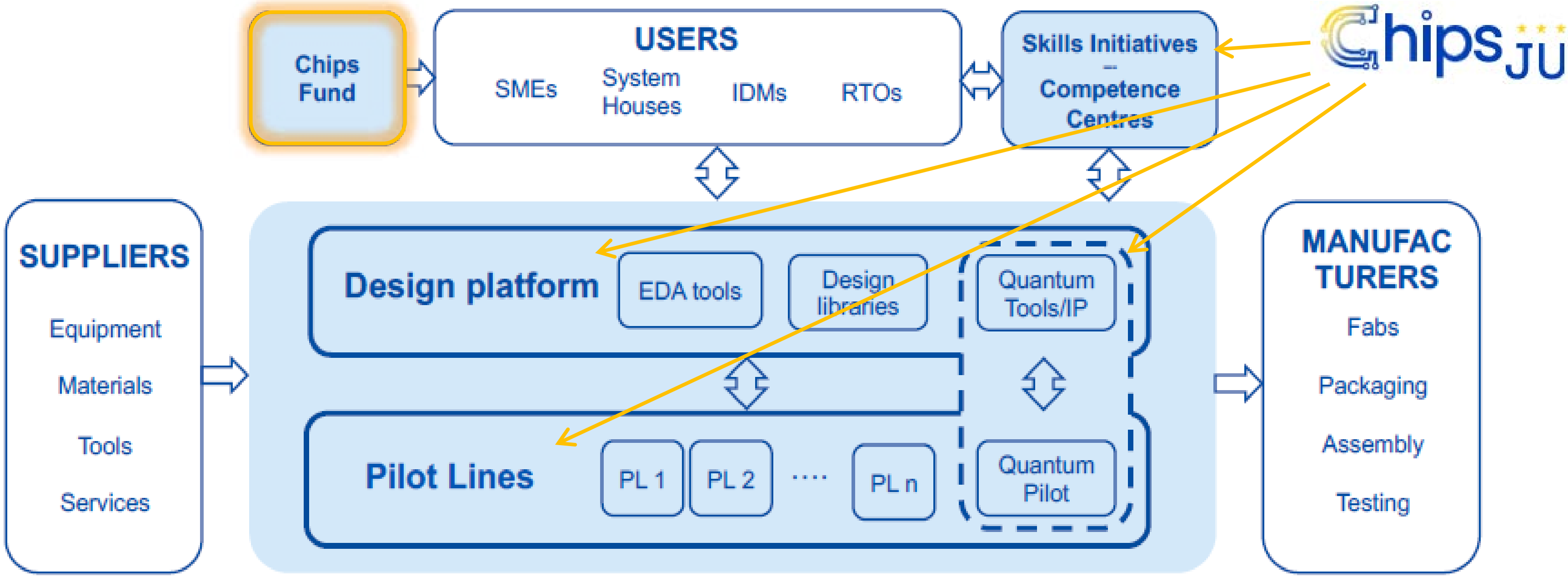
European Semiconductor Board

Chips for Europe Initiative

Security of Supply

Crisis response

Chips ACT/P1: Chips for EU - Objetivos



Chips ACT/P2: Security of Supply

Integrated Production Facility (IPF)

Vertically integrated first-of-a-kind facility which produce the chips they design and market

Open EU Foundry (OEF)

First-of-a-kind facility that (also) **produces chips** which are designed and marketed by **unrelated undertakings**

- **Qualification as first-of-a-kind facility:** Facility needs to offer innovation that is not yet present in the Union
- Clear **positive impact on the value chain** (security of supply and qualified workforce)
- **Security of supply:** guarantees not to be subject to extraterritorial application of public service obligations of third countries in a way that undermines the ability to accept priority rated orders
- Clear commitment to **invest in further innovation**

Chips ACT/P3: Crisis response

Monitoring stage

- Regular monitoring by Member States and update mechanism for alerts by stakeholders
- Board meetings with advisory participation of industry stakeholders and other relevant Union bodies

Crisis trigger

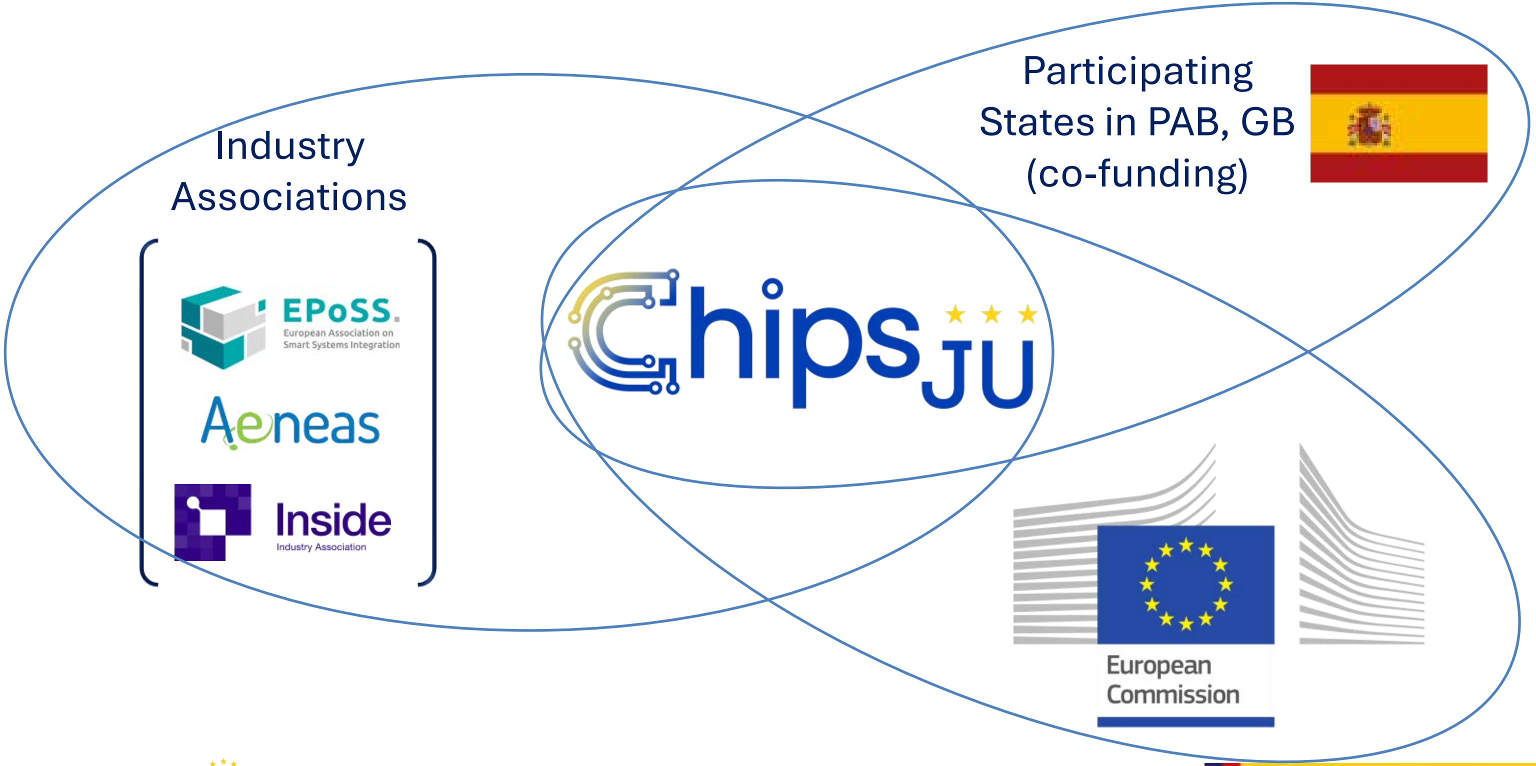
When **assessment of Commission provides evidence** of serious disruptions in the supply
- entailing significant negative effects on one or more important sectors, or
- preventing the repair and maintenance of essential products used by critical sectors

Commission implementing act

Crisis stage

- Emergency Toolbox activated: info gathering, priority orders, export control
- Intensified coordination in the European Semiconductor Board

Chips Joint Undertaking



Industry Associations

EPoSS European Association on Smart Systems Integration

Aeneas

Inside Industry Association

Chips JU

Participating States in PAB, GB (co-funding)

European Commission

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CDTI INNOVACIÓN

Chips JU – Member funtions

E C S

Strategic Research and Innovation Agenda 2025

ELECTRONIC COMPONENTS AND SYSTEMS

+

EPoSS.
European Association on Smart Systems Integration

Aeneas

Inside
Industry Association

Member States

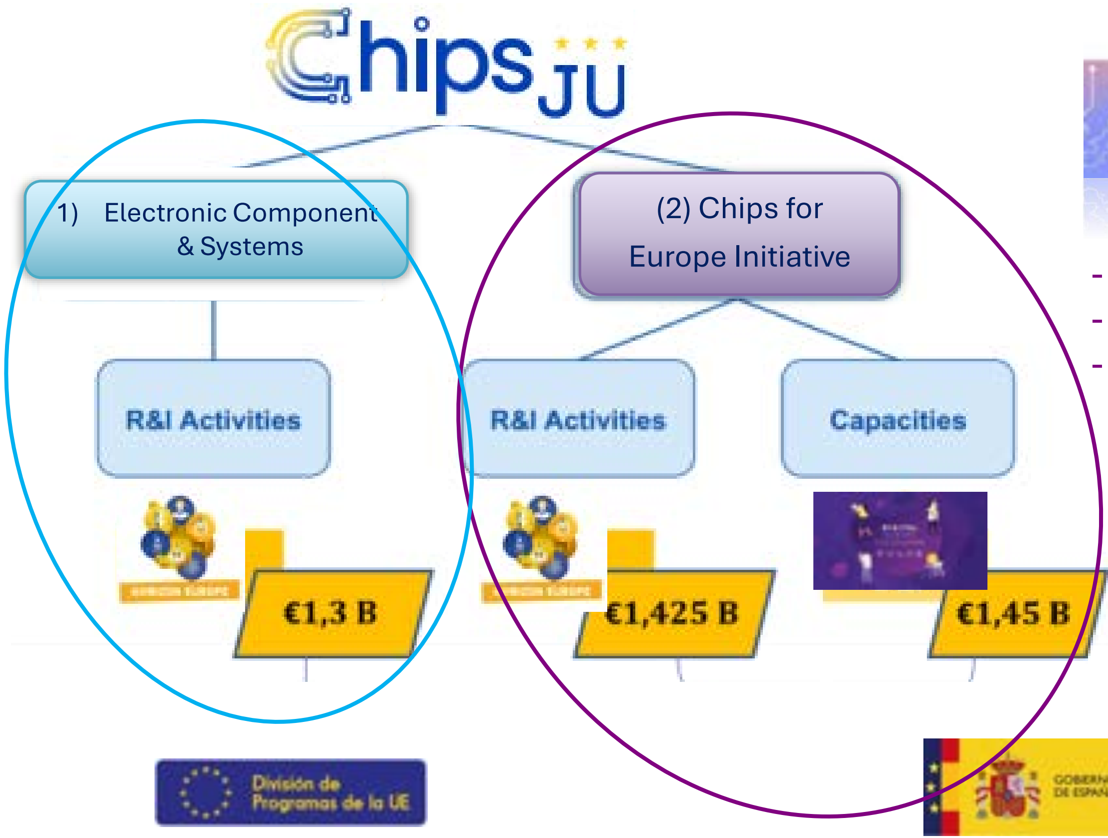
European Commission

=

Work Programme

Chips JU: Estructura

R & I
electronics



- Pilot lines
- Design Platform
- Competence Centers

Chips JU: Estructura MAWP-2025

R & I
electronics

1) Electronic Component & Systems

MAWP - Appendix 5 - ECS

(2) Chips for Europe Initiative

MAWP - Appendix 6 - CEI

- Pilot lines
- Design Platform
- Competence Centers

https://www.chips-ju.europa.eu/Documents/

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Chips JU: Programa de Trabajo 2025 (I)

Electronic Components & Systems

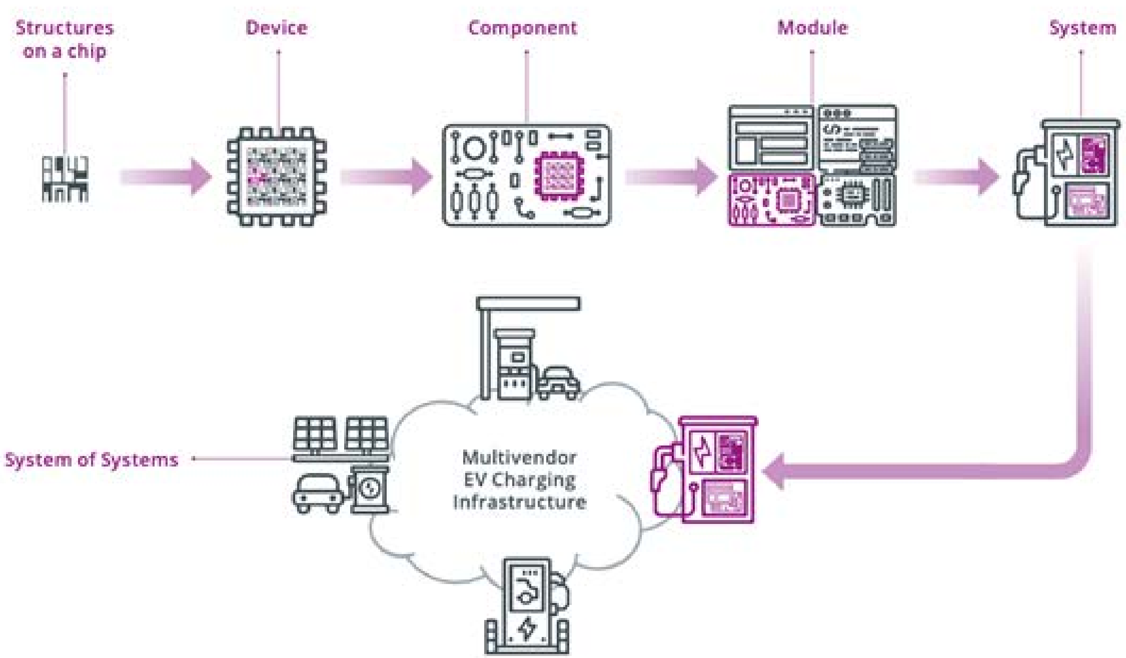
Call	Topic	Title	Budget (M€)
1- IA	HORIZON-JU-Chips-2025-IA	Global call according to SRIA 2024 (IA)	70
1- IA	HORIZON-JU-Chips-2025-IA-HIA	Heterogeneous integration for high-performance automotive computing	20
1- IA	HORIZON-JU-Chips-2025-IA FT1	RISC-V Automotive Hardware Platform	80
1- IA	HORIZON-JU-Chips-2025-IA FT2	AI-assisted Methods and Tools for Engineering Automation	20
2 - RIA	HORIZON-JU-Chips-2025-RIA	Global RIA call	40
3 -CSA	HORIZON-Chips-2025-CSA	Boosting R&I cooperation between EU and Japan on semiconductors	1

https://www.chips-ju.europa.eu/Documents/

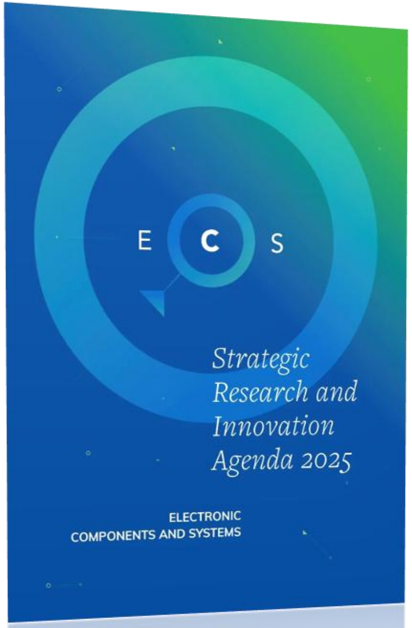
Fechas de cierre:
- HORIZON-Chips-2025-CSA (1 fase): 17/9/2025
- Resto: 1ª FASE: 29/4/2025, 2ª FASE: 17/9/2025

(1) Electronic Component & Systems (ECS)

EXAMPLE OF ELECTRONIC COMPONENTS AND SYSTEMS



(1) ECS: Global IA & RIA



E C S

Strategic Research and Innovation Agenda 2025

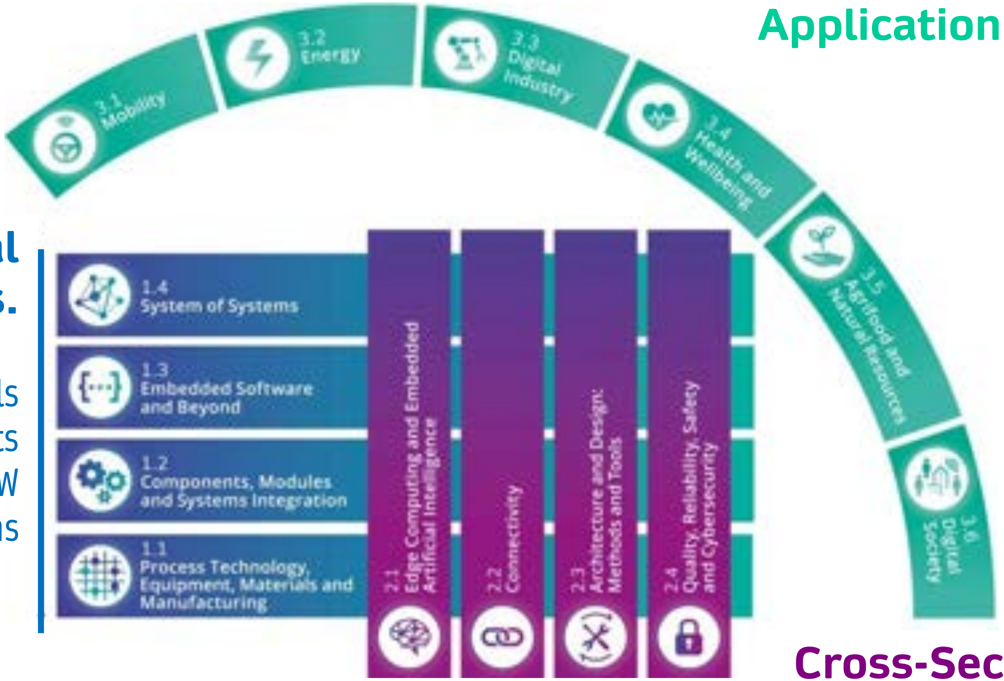
ELECTRONIC COMPONENTS AND SYSTEMS

3.1 - Mobility

- **Major challenge 1:** SDV hardware platforms: modular, scalable, flexible, safe & secure
- **Major challenge 2**: SW platforms for SDV of the future: modular, scalable, re-usable, flexible, safe & secure, supporting edge2cloud applications
- **Major challenge 3:** Green deal: enable climate and energy optimal mobility
- **Major challenge 4:** Digitalisation: affordable and safe automated and connected mobility for passengers and freight
- **Major challenge 5:** Edge2cloud mobility applications: added end-user value in mobility
- **Major challenge 6:** AI enabled engineering tool chain: agile collaborative SDV SW development and SDV as well as ADAS/AD validation

https://ecssria.eu/2025

(1) ECS: Global IA & RIA



Foundational Techs.

Process/materials
Components
Embedded SW
Systems-of-Systems

Application Areas

Mobility
Energy
Industry
Health
Agrifood
Society

AI/Edge
Connect
Tools/Design
Cybersec.

Cross-Sectional Techs.

(1) ECS: Focus topics

HORIZON-JU-Chips-2025-IA-HIA: Heterogeneous integration for high-performance automotive computing

Integration of different chip components (chiplets) to create powerful and efficient automotive computing systems. It aims to develop innovative packaging and interconnect technologies, particularly using 2.5D and 3D integration, to enable higher performance while managing complexity and cost for advanced automotive applications.

HORIZON-JU-Chips-2025-IA FT1: RISC-V Automotive Hardware Platform

Establish a robust hardware platform for automotive applications based on the open-source RISC-V instruction set architecture (ISA). It promotes the development of high-performance RISC-V processors, accelerators, and associated tools to enable innovation and European leadership in automotive computing

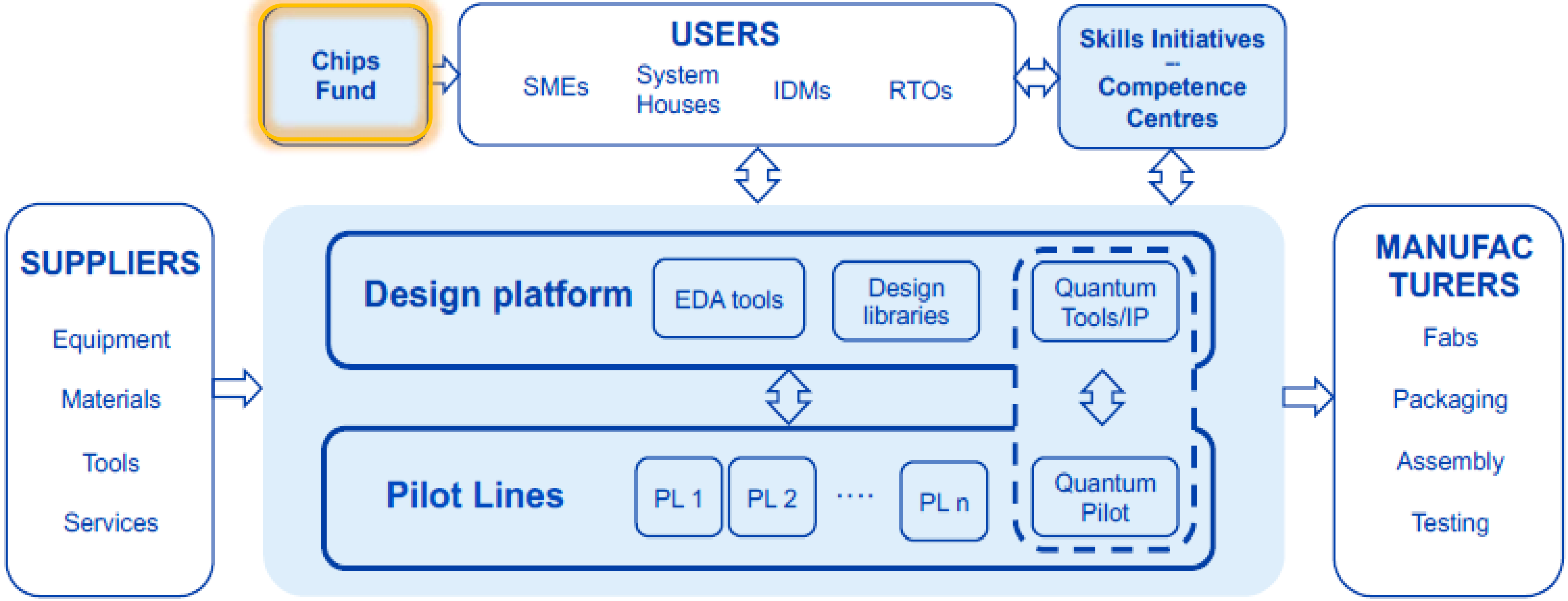
HORIZON-JU-Chips-2025-IA FT2: AI-assisted Methods and Tools for Engineering Automation

Developing and using AI-powered methods and tools to automate software engineering tasks, particularly for complex automotive electronic systems. It aims to improve development efficiency, reduce costs, and enhance the reliability of software-defined vehicles using AI for design, testing, and validation, leveraging European standards and methods.

(1) ECS: Focus topics

Condition	*HORIZON-JU-Chips-2025-IA-HIA: Heterogeneous Integration*	*HORIZON-JU-Chips-2025-IA FT1: RISC-V Automotive Hardware Platform*	*HORIZON-JU-Chips-2025-IA FT2: AI-assisted Methods & Tools*
Type of Action	Innovation Action (IA)	Innovation Action (IA)	Innovation Action (IA)
Estimated JU Expenditure	20 Million Euro	80 Million Euro	20 Million Euro
Mode	One-Stage Call	Two-Stage Call	Two-Stage Call
Call Launch Date	04 Mar 2025	04 Mar 2025	04 Mar 2025
Deadline Project Outline (PO)	N/A	29 Apr 2025 at 17:00 Brussels Time	29 Apr 2025 at 17:00 Brussels Time
Deadline Full Project Proposal (FPP)	29 Apr 2025 at 17:00 Brussels Time	17 Sep 2025 at 17:00 Brussels Time	17 Sep 2025 at 17:00 Brussels Time
Technology Readiness Level (TRL)	To cover from the present state to TRL 7-8 at the end of the project.	The activities must have their centre of gravity at TRL 7-8 at the end of the project.	To cover from the present state to TRL 6-7 at the end of the project.
Size Limit	15 Participants	25 Participants	40 Participants

(2) Chips for Europe Initiative



Chips JU: Programa de Trabajo 2025 (II)

Chips for Europe Initiative

Call	Topic	Title	M€	Deadline
Design Platform	Call for Tenders*	Cloud platform for the European Design Platform	15	n.a.
Design Platform	DIGITAL-JU-Chips-2025-CSA-DET*	Set-up and integration of Design Enablement Teams	5	TBD
Design Platform	HORIZON-JU-Chips-2025-RIA-SUP	Support for start-ups and SMEs	220	17-sep-25
Design Platform	HORIZON-JU-Chips-2025-IA-EDA**	Open-source EDA tools development	20	29/4/25, 17/9/25
Design Platform	HORIZON-JU-Chips-2025-CSA	A Pan-European infrastructure for Chips Design Innovation	12	29 Apr-25
AI Chips	HORIZON-Chips-2025-1-IA-LEAI**	Low-power Edge AI Chips	20	29/4/25, 17/9/25
Substrates	DIGITAL-JU-Chips-2025-SG-SSOI*	Accelerator for Advanced Strained Silicon on Insulator Substrates	30	17-sep-25
Quantum	HORIZON-JU-Chips-2025-FPA-QAC3	Establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilot Lines	0	TBD
Quantum	HORIZON-JU-Chips-2025-SGA-QAC1	Supporting developing Quantum Chip Technology for stability Pilot Lines	50	TBD
Quantum	HORIZON-JU-Chips-2025-SGA-QAC2	Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot Line	20	TBD

https://www.chips-ju.europa.eu/Documents/

(*) Convocatorias fuera de Horizonte Europa (Licitaciones y Programa DEP)
(**) Líneas en 2 fases: 1ª FASE: 29/4/2025, 2ª FASE: 17/9/2025

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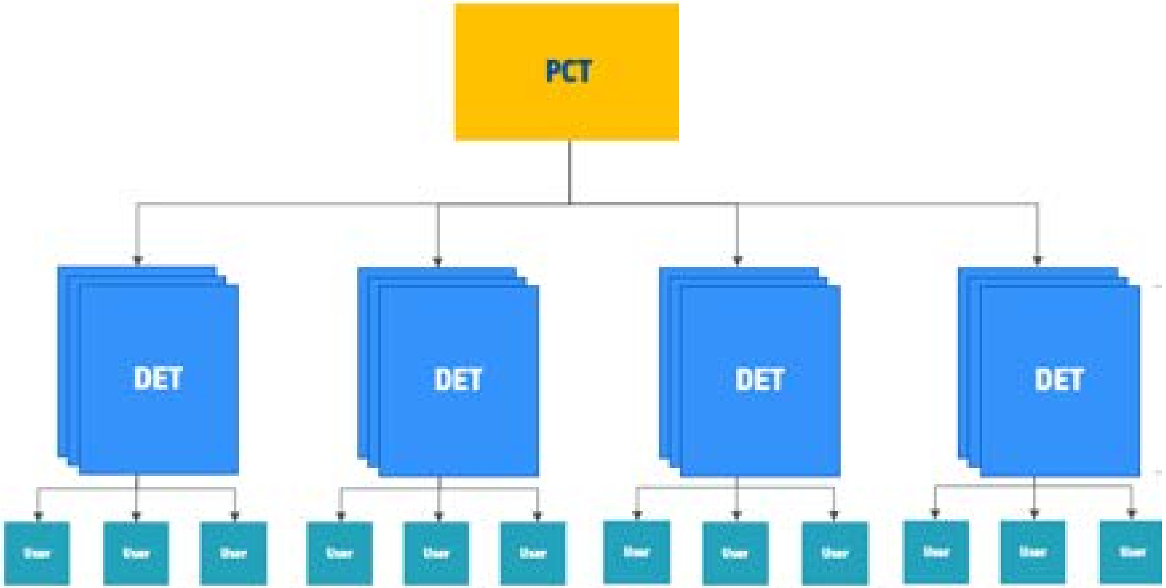
(2) Horizon Europe / CEI

Topic Code	Specific Conditions
HORIZON-JU-Chips-2025-RIA-SUP	- Beneficiaries may provide financial support to third parties (grants). - Maximum amount to be granted to each third party is EUR 8 million. - Subject to participation restrictions for the protection of European communication networks.
HORIZON-JU-Chips-2025-IA-EDA	- TRL 7/8 - For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding. - Subject to restrictions for the protection of European communication networks. - Maximum Contribution per partner: 40% of the total EU funding. - Size limit: 30 Participants
HORIZON-JU-Chips-2025-CSA	- Subject to restrictions for the protection of European communication networks
HORIZON-Chips-2025-1-IA-LEAI	- For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding. - Subject to restrictions for the protection of European communication networks.
HORIZON-JU-Chips-2025-FPA-QAC3	- For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding. - Subject to restrictions for the protection of European communication networks. - Size limit: 50 Participants
HORIZON-JU-Chips-2025-SGA-QAC1	- For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding. - Subject to restrictions for the protection of European communication networks. - Size limit: 50 Participants - Max Contribution per partner: 40% of the total EU funding.
HORIZON-JU-Chips-2025-SGA-QAC2	- For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding. - Subject to restrictions for the protection of European communication networks. - Size limit: 50 Participants - Max Contribution per partner: 40% of the total EU funding.

(2) Design platform



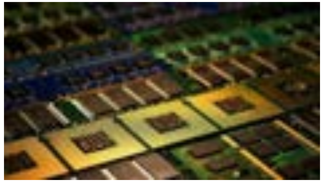
Platform Coordination Team (PCT)

Coordination of the Design Platform
Link to Chips for Europe Initiative Infrastructure
Negotiation of framework agreements with vendors
Definition of common look and feel across Design Enablement Teams
Quality assurance

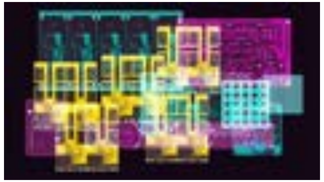
Design Enablement Teams (DETs)

Application engineering support to users
Hosting of cloud instance
Supporting users in setting up their design environment and design flows
Interface with foundries for prototyping
Supply chain management for prototypes and volume products

(2) Design platform



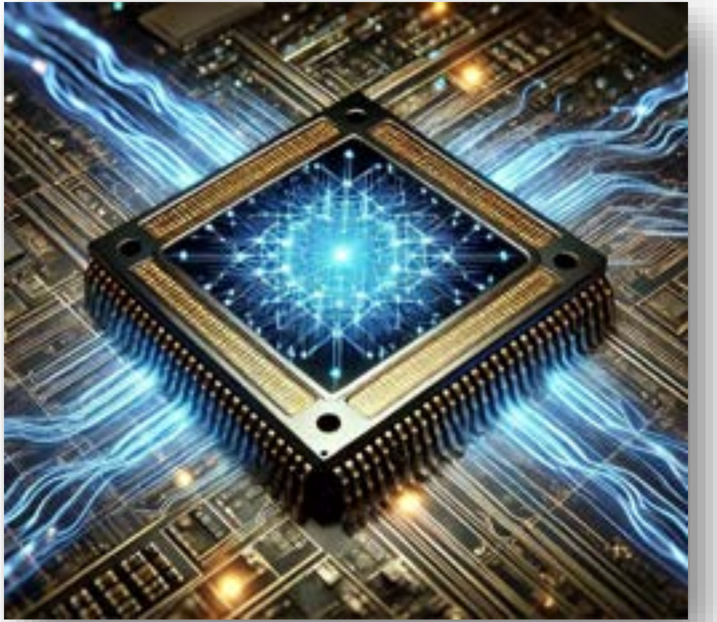
HORIZON-JU-Chips-2025-RIA-SUP: Support for start-ups and SMEs: This call focuses on running an incubation and acceleration program to support European startups and SMEs involved in chip design. Services, including financial support (grants), to help these companies overcome barriers to entry and scale up. Selection considers both technical merit and business viability. It also sets out a Start-up support programme.



HORIZON-JU-Chips-2025-IA-EDA: Open-source EDA tools development: Open-source Electronic Design Automation (EDA) tools, bridging the gap between existing open-source resources and commercial EDA tools. Streams: (i) digital SoC design, (ii) analogue and mixed-signal design, or (iii) productivity, interoperability, and verification. The goal is to improve tool quality, performance, and user experience, including integration with the Design Platform and foundries.

HORIZON-JU-Chips-2025-CSA: A Pan-European infrastructure for Chips Design Innovation: This call seeks to establish a pan-European platform (building upon and extending EUROPRACTICE) to provide open access to chip design and fabrication services. The scope includes creating a platform for the European design ecosystem, promoting the sharing of Process Design Kits (PDKs), streamlining access to EDA tools, enhancing workforce skills, facilitating prototyping, and offering extensive training resources. A key objective is the *integration* of EUROPRACTICE services into the Chip Act's Design Platform.

(2) Pilot Lines: Quantum

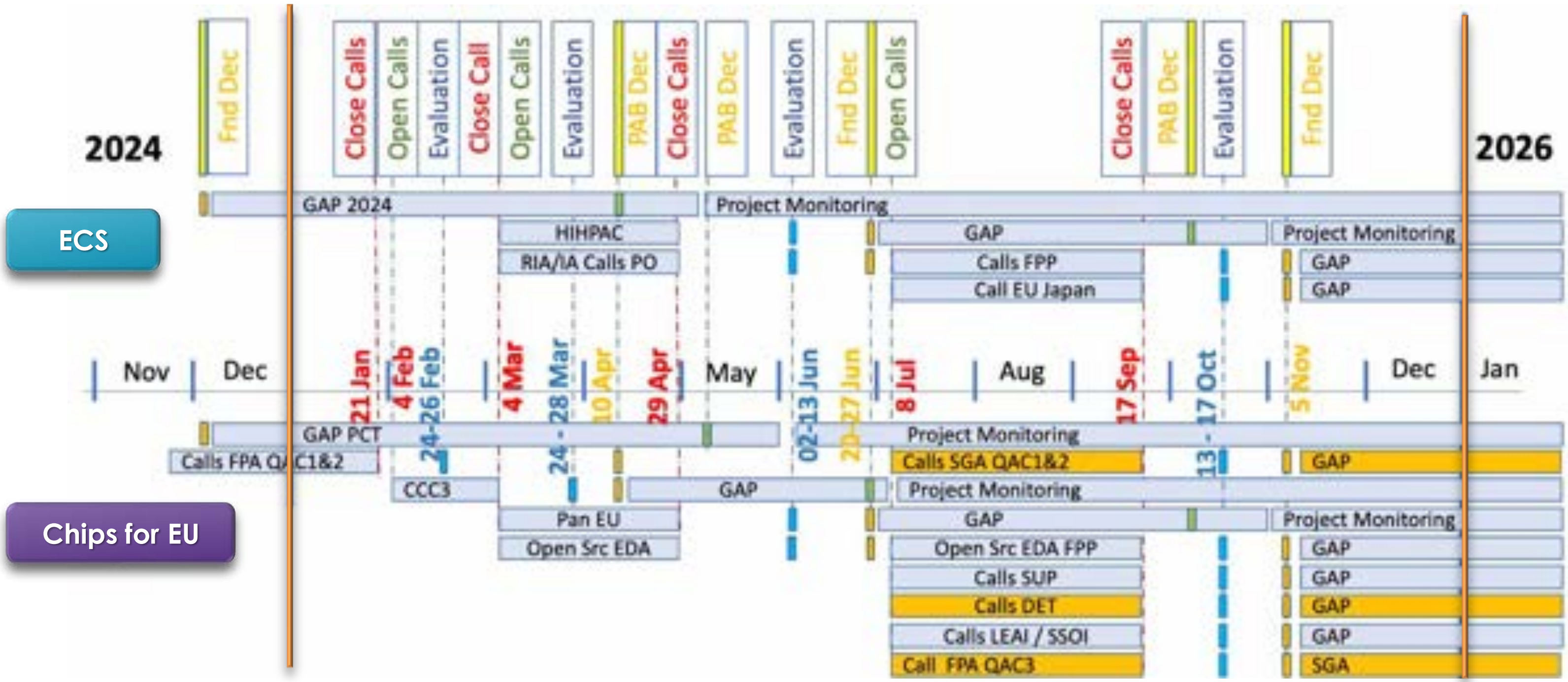


HORIZON-JU-Chips-2025-FPA-QAC3: Establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilot Lines. The focus is on stability and preparing the technologies for industrialization. The FPAs will cover a range of quantum technologies (superconducting, photonic, semiconducting, diamond-based, or neutral atoms) and lay out a plan for multiple Specific Grant Agreements (SGAs)

HORIZON-JU-Chips-2025-SGA-QAC1: Supporting developing Quantum Chip Technology for stability Pilot Lines. Developing scalable production processes, integrating PDKs, enhancing technology and manufacturing (TRL 6), establishing standardized methodologies, and demonstrating stable production capabilities

HORIZON-JU-Chips-2025-SGA-QAC2: Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot Line Includes developing scalable and efficient production capacities, integrating PDKs, and establishing standardized methodologies, all tailored to the unique requirements of trapped-ion technology.

WP2025: Open Calls



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Successful proposal

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GOBIERNO DE ESPAÑA MINISTERIO DE CIENCIA, INNOVACIÓN Y UNIVERSIDADES CDTI INNOVACIÓN

Participation: Successful proposal

EXCELENCE

- Objectives and ambition (+ **State-of-Art**)
- Metodology

IMPACT

Output > Outcome > Impact

IMPLEMENTATION

- Work plan
- Capacity of participants and consortium

Success: Idea

https://ecssria.eu/2025

Chips JU Documentation

https://www.chips-ju.europa.eu/Projects/

Previous projects (ECSEL / KDT /ChipsJU)

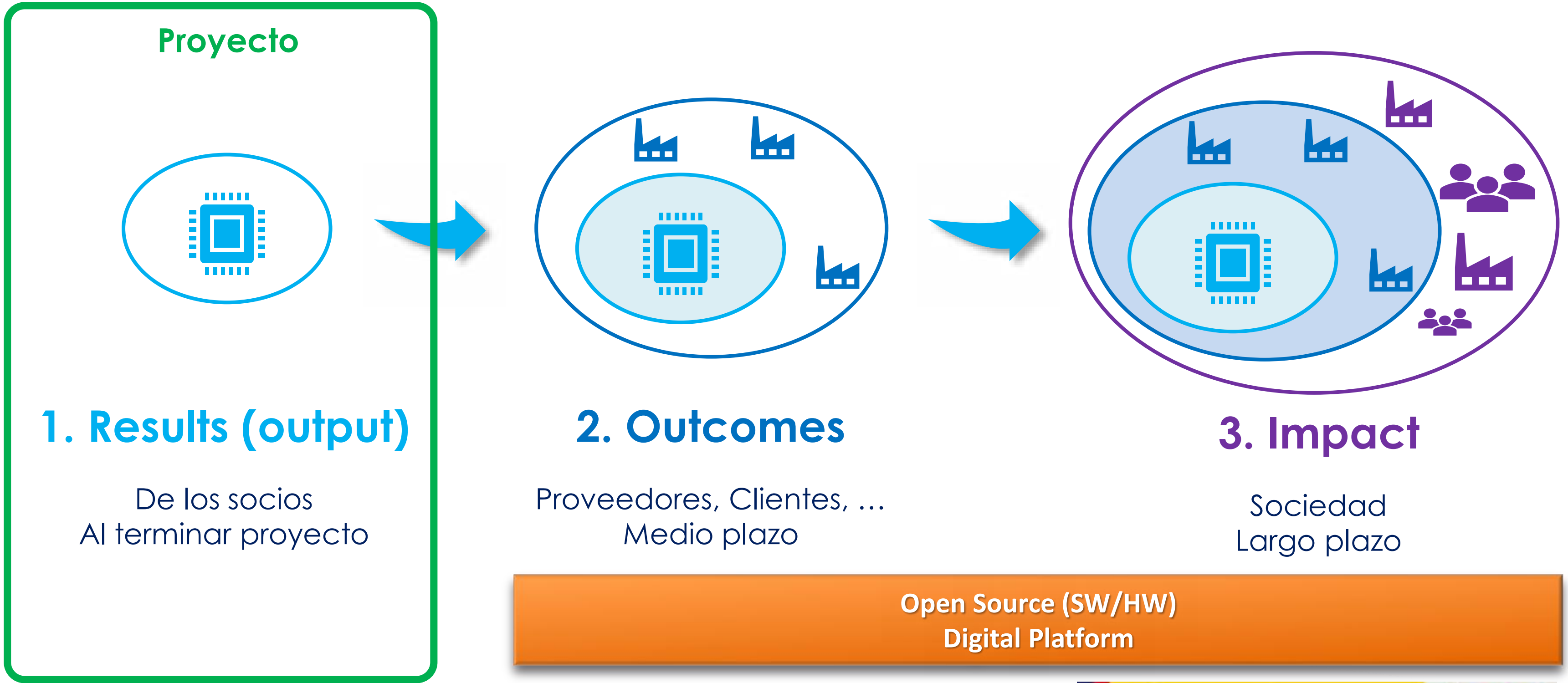
Success: Excelencia

- **Estado del arte:** Formato de "*storytelling*" Resumir en 1-2 frases el conocimiento actual y señalar el vacío que tu propuesta llenará. Destacar la innovación del nuevo enfoque:

  "Aunque [tecnología/método actual] ha avanzado, sigue sin resolver [limitación]. Proponemos [concepto/método], una solución pionera que supera las limitaciones existentes."

- **Metodología:**
  - Conceptos, supuestos y modelos utilizados para alcanzar los objetivos planteados.
  - Incluir aspectos horizontales.

Success: Impact



Proyecto

1. Results (output)

De los socios
Al terminar proyecto

2. Outcomes

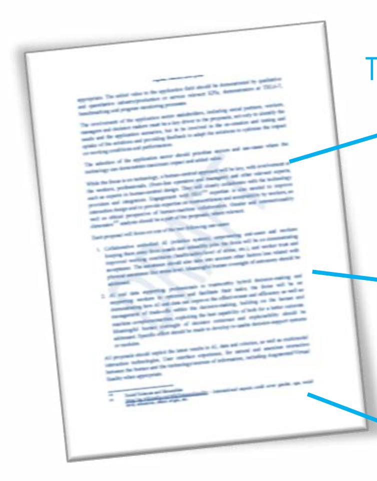
Proveedores, Clientes, …
Medio plazo

3. Impact

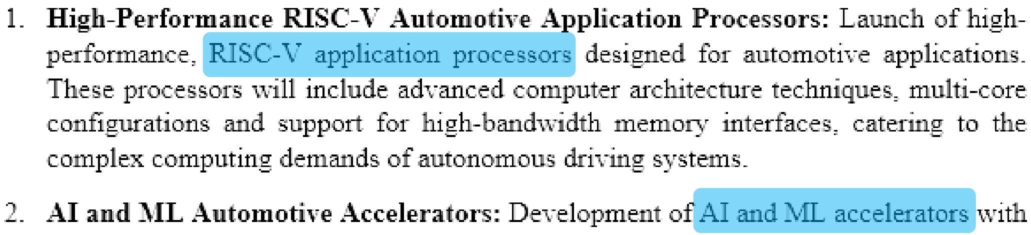
Sociedad
Largo plazo

Open Source (SW/HW)
Digital Platform

Success: Implementation/Consortium



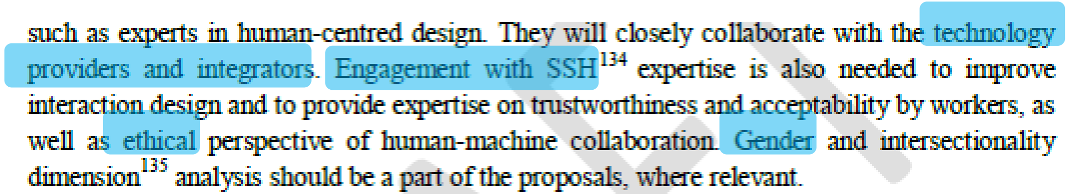
Tecnologías



1. **High-Performance RISC-V Automotive Application Processors:** Launch of high-performance, RISC-V application processors designed for automotive applications. These processors will include advanced computer architecture techniques, multi-core configurations and support for high-bandwidth memory interfaces, catering to the complex computing demands of autonomous driving systems.
2. **AI and ML Automotive Accelerators:** Development of AI and ML accelerators with

Skills / SSH / ética /…

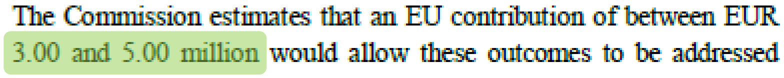
Ethics @ AI



such as experts in human-centred design. They will closely collaborate with the technology providers and integrators. Engagement with SSH[134] expertise is also needed to improve interaction design and to provide expertise on trustworthiness and acceptability by workers, as well as ethical perspective of human-machine collaboration. Gender and intersectionality dimension[135] analysis should be a part of the proposals, where relevant.

Usuarios / validación

In all proposals, user industries are expected to play a major role in the requirement and validation phases.



The Commission estimates that an EU contribution of between EUR 3.00 and 5.00 million would allow these outcomes to be addressed

Número de socios **34,2 RIA / 43,5 IA**

En ChipsJU

Chips JU: Cofinanciación

European Commission

Type of Beneficiary	General IA	Focus Topic IA	General RIA	CSA
Large Enterprise	20%	25%	25%	100%
SME	30%	35%	35%	100%
University/Other (not for profit)	35%	35%	35%	100%

* Los porcentajes pueden variar para líneas específicas

EUROPEAN CHIPS ACT

GOBIERNO DE ESPAÑA
MINISTERIO DE TRANSFORMACIÓN DIGITAL Y FUNCIÓN PÚBLICA

GOBIERNO DE ESPAÑA
MINISTERIO DE TRANSFORMACIÓN DIGITAL Y FUNCIÓN PÚBLICA

Enterprise / SME

\+

GOBIERNO DE ESPAÑA
MINISTERIO DE CIENCIA, INNOVACIÓN Y UNIVERSIDADES

University/Other (not for profit)

Chips JU: Puntos Nacionales de Contacto (NCP)

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Conclusiones

- Electrónica / semiconductores en distintos partenariados
- Importancia de la industria
- Apoyarse en los NCPs

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+ info sobre programas y ayudas
para la
internacionalización de la I+D+I española

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